Claims

[c1] 1.An electrostatic discharge (ESD) protection circuit, comprising:an N substrate having four separate wells, including a high voltage (HV) N-well arranged between a first HV P-well and a second HV P-well and a third HV P-well, wherein the first HV P-well comprises a first P+ region and the second HV P-well comprises a second P+ region, wherein the third HV P-well exists apart in the N substrate and is separate from the other three wells, the HV N-well further comprising: a first N- region and a first N+ region disposed within and encompassed by the first N- region, and the third HV P-well further comprising: a third and a fourth P+ regions near both sides of the HV P-well; a second N- region separate from and between the third and fourth P+ regions; and a second N+ region disposed within and encompassed by the second N- region.

[c2] 2. The ESD protection circuit of claim 1, wherein a spacing exists between the second N- region and the second N+ region.

[c3] 3. The ESD protection circuit of claim 2, wherein the spacing is about 0.5 microns to about 5 microns.

[c4] 4. An electrostatic discharge (ESD) protection circuit, comprising:a P substrate having four separate wells, including a first high voltage (HV) N-well arranged between a first HV P-well and a second HV P-well and a second HV N-well, wherein the first HV P-well comprises a first P+ region and the second HV P-well comprises a second P+ region, wherein the second HV N-well exists apart in the P substrate and is separate from the other three wells, the first HV N-well further comprising: a first N- region and a first N+ region disposed within and encompassed by the first N- region, and the second HV N-well further comprising: a second and a third N+ regions near both sides of the HV N-well; a first P- region separate from and between the second and third N+ regions; and a third P+ region disposed within and encompassed by the first P- region.

[c5] 5. The ESD protection circuit of claim 4, wherein a spacing exists between the first P- region and the third P+ region.

[c6] 6. The ESD protection circuit of claim 5, wherein the spacing is about 0.5

microns to about 5 microns.